Claims:

1. A timing circuit for generating clock signals, comprising:

an acquisition digital phase locked loop with a wide capture range for closely following an input signal and with its associated disturbances; and

an output digital phase locked loop having a slow response relative to said acquisition phase locked loop, said output digital phase locked loop tracking a digital output of said acquisition phase locked loop to generate an output signal for the timing circuit.

2. A timing circuit as claimed in claim 1, wherein said acquisition digital phase locked loop and said output phase locked loop include digital low pass filters, said digital low pass filter in said acquisition digital phase locked loop having a higher cut-off frequency than said digital low pass filter in said output phase locked loop.

3. A timing circuit as claimed in claim 2, wherein said digital low pass filter in said acquisition digital phase locked loop has a sufficiently high cut-off frequency to ensure that the output closely tracks the input signal and its associated error components.

4. A timing circuit as claimed in claim 3, wherein said digital low pass filter in said output digital phase locked loop has a sufficiently low cut-off frequency to ensure that the output tracks the output of said acquisition digital phase locked loop signal without the associated error components present in the input signal.

5. A timing circuit as claimed in claim 1, comprising a plurality of said acquisition digital phase locked loops receiving respective input signals, each said acquisition digital phase locked loops being connected through a functional circuit to said output phase locked loop.

6. A timing circuit as claimed in claim 5, wherein said functional circuit is a multiplexer to select one of the outputs of said acquisition digital phase locked loops.

7. A timing circuit as claimed in claim 6, wherein said functional circuit is an adder to combine the outputs of said acquisition digital phase locked loops to provide an average.

8. A timing circuit as claimed in claim 7, wherein said adder generates a weighted average.

9. A timing circuit as claimed in claim 5, wherein functional circuit derives an output from the outputs of said acquisition digital phase locked loops according to mathematical equation.

10. A timing circuit as claimed in claim 5, wherein inputs of said acquisition digital phase locked loops are connected through respective multiplexers to a plurality of inputs and a crystal oscillator.

11. A method of generating clock signals from an input signal subject to errors, comprising:

tracking the input signal and its error components with an acquisition digital phase locked loop to produce a digital output signal, and

tracking said digital output signal with an output digital phase locked loop with a slow response relative to said acquisition digital phase locked loop so as to eliminate said error components.

12. A method as claimed in claim 11, wherein said acquisition digital phase locked loop has a digital filter with a high cut off frequency relative to the cut-off frequency of a digital filter in said output digital phase locked loop.

13. A method as claimed in claim 12, wherein a plurality of input signals are tracked with respective said acquisition digital phase locked loops to produce a plurality of digital output signals which are passed through a functional block for tracking with said output digital phase locked loop.

14. A method as claimed in claim 13, wherein said functional block permits selection one of the digital outputs of said acquisition digital phase locked loops.

15. A method as claimed in claim 13, wherein said functional block combines said digital outputs of said acquisition digital phase locked loops to produce an average.

16. A method as claimed in claim 15, wherein said average is a weighted average.

17. A method as claimed in claim 13, wherein one of a plurality of input signals are selectable for input to each of said acquisition phase locked loops.

18. A method as claimed in claim 17, wherein one of said input signals is derived form a crystal oscillator for test purposes.

19. A method as claimed in claim 12, wherein said filter in said acquisition phase locked loop as a cut-off frequency of a few hundred Hertz.

20. A method as claimed in claim 14, wherein one of said input signals provides a back-up signal for use in the event of failure of a principal reference signal.